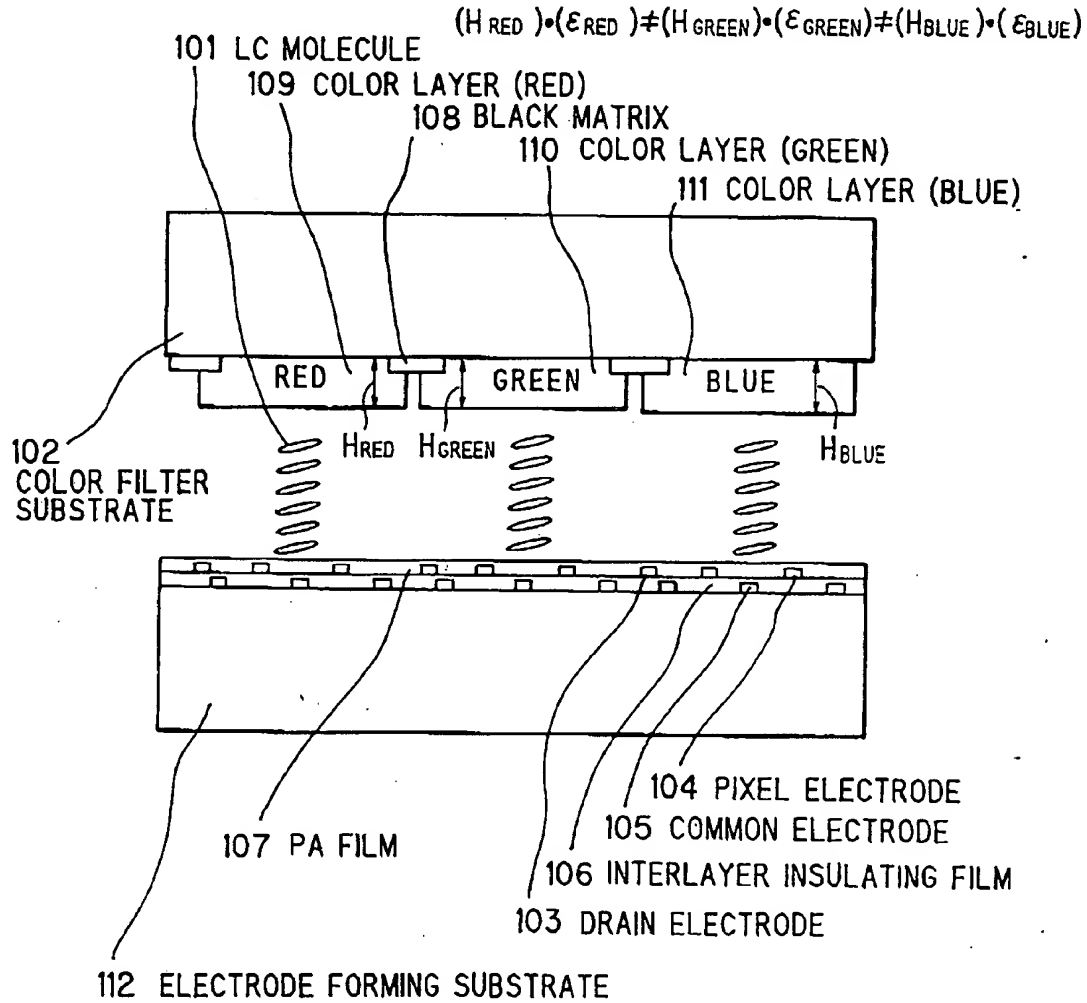


FIG. 1 PRIOR ART



The diagram illustrates a cross-section of a liquid crystal display (LCD) panel. The top layer is labeled 101 LC MOLECULE. Below it are three color layers: 109 COLOR LAYER (RED), 110 COLOR LAYER (GREEN), and 111 COLOR LAYER (BLUE). These are separated by a 108 BLACK MATRIX. The entire assembly sits on a 102 COLOR FILTER SUBSTRATE. Below the color filter substrate are three vertical springs representing spacers, labeled H_{RED}, H_{GREEN}, and H_{BLUE}. At the bottom is a 112 ELECTRODE FORMING SUBSTRATE. On this substrate are several electrodes: 107 PA FILM, 103 DRAIN ELECTRODE, 104 PIXEL ELECTRODE, and 105 COMMON ELECTRODE. An 106 INTERLAYER INSULATING FILM is also shown.

$(H_{\text{RED}}) \cdot (\epsilon_{\text{RED}}) = (H_{\text{GREEN}}) \cdot (\epsilon_{\text{GREEN}}) = (H_{\text{BLUE}}) \cdot (\epsilon_{\text{BLUE}})$

303 GATE ELECTRODE

305 TFT ELEMENT

304 DRAIN ELECTRODE

302 LC CAPACITANCE + COLOR LAYER CAPACITANCE

COLOR LAYER R OF COLOR FILTER

COLOR LAYER G OF COLOR FILTER

COLOR LAYER B OF COLOR FILTER

301

306

307

309

308 HOLDING CAPACITANCE OF TFT ELEMENT

Diagram illustrating the timing of the Drain Voltage (V_D) and the Color Layer signals (R, G, B) for a 3-phase 1T1C TFT-LCD driver.

The vertical axis represents the Drain Voltage (V_D), with levels V_1 , V_2 , and V_3 marked. The horizontal axis represents time.

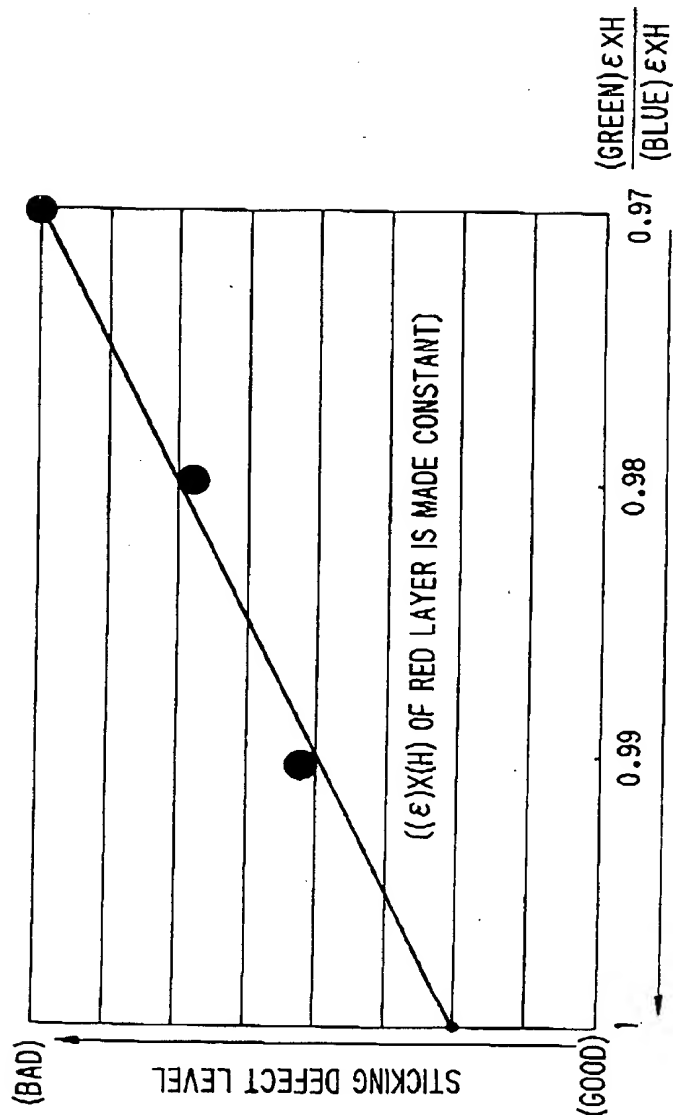
The signals shown are:

- COLOR LAYER R OF COLOR FILTER**: A square wave signal that is high during the V_1 phase and low during the V_2 and V_3 phases.
- COLOR LAYER G OF COLOR FILTER**: A square wave signal that is high during the V_2 phase and low during the V_1 and V_3 phases.
- COLOR LAYER B OF COLOR FILTER**: A square wave signal that is high during the V_3 phase and low during the V_1 and V_2 phases.
- DRAIN VOLTAGE WAVEFORM**: A square wave signal that is high during the V_1 phase, low during the V_2 phase, and high during the V_3 phase.

The relationship between the voltage levels is indicated by the inequality:

$$V_3 > V_2 > V_1$$

FIG.6



DIRECTION WHERE "(COLOR-LAYER STATIC CAPACITANCE) + (LC STATIC CAPACITANCE)" OF RESPECTIVE COLOR LAYERS OF COLOR FILTER BECOMES EQUAL

(AT ABSCISSA POINT = 1, "(COLOR-LAYER STATIC CAPACITANCE) + (LC STATIC CAPACITANCE)" OF RESPECTIVE COLOR LAYERS ARE EQUAL)

FIG. 7

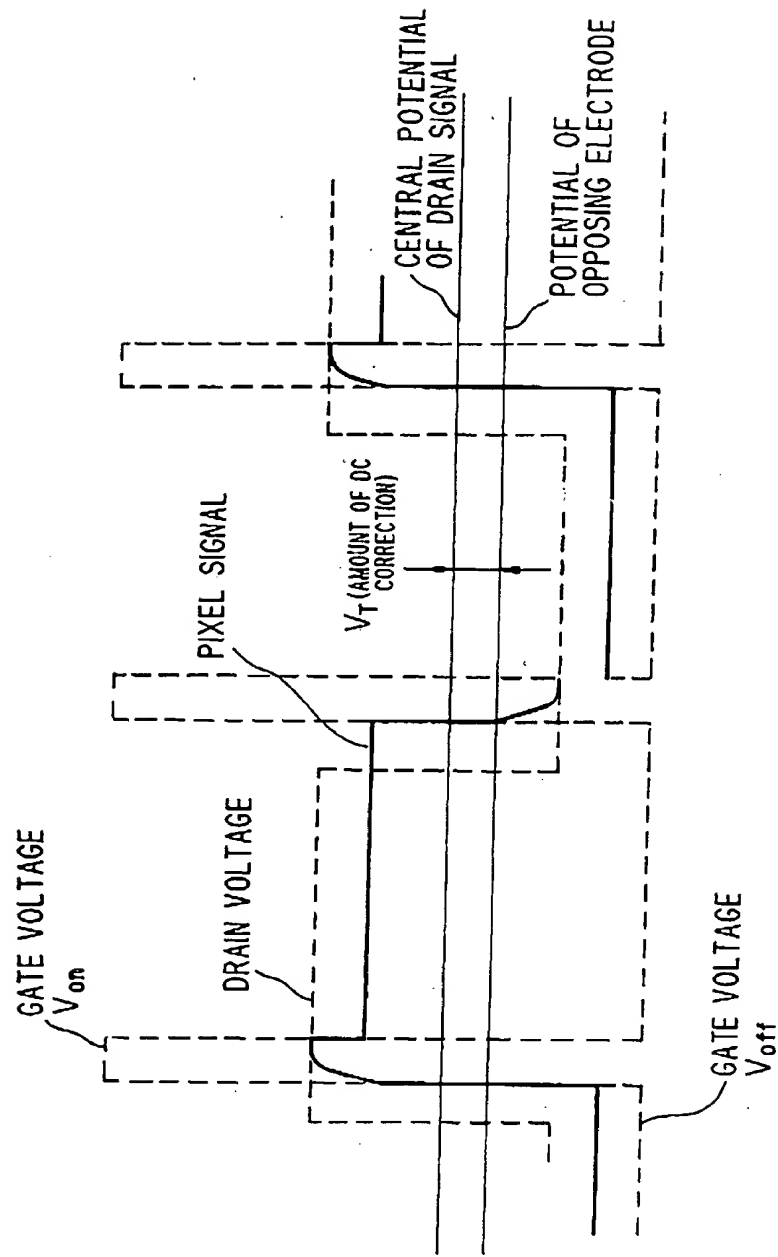


FIG. 8

